MODELING THERMAL AND ELECTRICAL PROCESSES IN A SEMICONDUCTOR MODULE WITH A TEMPERATURE CONSTRAINT

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A method of combined investigation is proposed for thermal and electrical process in semiconductor modules with a temperature constraint.

FORMULATION OF THE PROBLEM

One method of improving the technicoeconomic parameters of output stages of power transducers is related to the development of powerful transistor gates. The rise in their power is accomplished by producing multibase, multiemitter structures [1], as well as by parallel connection of transistors [2], etc. A power increase can cause dangerous overheating of the whole transducer or overheating of the separate elements when the transistors are connected in parallel. All this results in the need to support apparatus by special systems of thermal restriction, cooling, thermostatting, etc.

One method of supporting a normal thermal regime of a module with an effective utilization of transistors is thermal constraint of the device [3] by using control of the power of the whole apparatus, group of elements, or each element individually. Thermal feedback can be realized by using different regulators (relays, positional, etc.) connected into the control (for instance, base) or power loop of the electronic apparatus.

A joint consideration of the thermal and electrical processes in the object and the regulator is needed to analyze the operation of such instruments.

The mathematical description reduces to three interrelated systems of equations: 1) for thermal processes in the devices themselves; 2) sensor heat transfer; 3) for electrical processes in the power stages of regulator operation with the actuator.

Mathematical modeling of thermal processes in different electrical engineering apparatus as well as the description of sensor operation and of regulator operation with an actuator are presented in [4, 5].

OBJECT OF THE INVESTIGATION

Let us examine the operation of an apparatus representing a parallel assembly of power transistors with a thermal constraint. The simplest version of a circuit with a temperature constraint is shown in Fig. 1a. According to the circuit, the input signal from the source E_b is delivered to the base of the transistor T through a voltage divider consisting of the resistance R_e in the emitter loop and R_b in base loop. The magnitude of the current through the load can be controlled by changing the relationship between their values. A thermal resistor (posistor) with nonlinear characteristic (Fig. 1b) is selected as resistor R_b. Upon reaching a given temperature level T_{cr} (critical), governed by the posistor properties, its resistance increases sharply, which causes growth of the input resistance, diminution of the base current and the current I_c through the load, and in fact, disconnection of the device. To obtain high gain, the cells are often combined in a Darlington circuit [6] with two transistors (Fig. 1c).

In its construction a parallel assembly consists of an array of transistors 2 (Fig. 2a) arranged on a common chassis base 1 equipped with a cooling system 7 (a radiator in this case). The array has the housing 3 to which the molybdenum substrate 4 with its mounted transistor crystal 5 is fastened. The posistor 6 (temperature sensor) can be mounted at any place in the device, on the crystal, the molybdenum substrate or on the device chassis.

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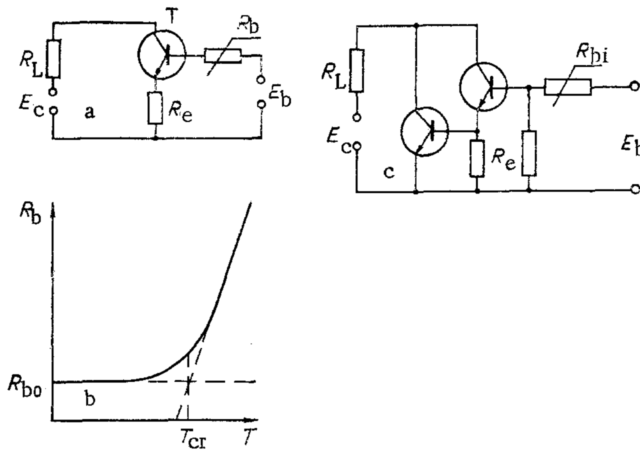

Fig. 1. Circuit diagrams of power stages of transistor gates with a thermal constraint (a, c) and temperature dependence of the posistor resistance (b).

A number of questions associated with the solution of structural, technological, thermophysical, electrotechnical and other problems. To realize them and the optimal design of both the individual arrays and their assembly as a whole, all these processes must be investigated interconnectedly.

PHYSICOMATHEMATICAL MODEL

At this time there are several methods of describing transistor operation [6, 7]. One of the most widespread is the classical Ebers—Moll model [1] according to which the electrical processes in the transistor are described by the following system of equations

$$\frac{E_b}{R_{bi}} = (1-\alpha_{Ni})\, I'_{e0i}\,(e^{U_{ei}/\varphi_{Ti}}-1) + (1-\alpha_{Ii})\, I'_{c0i}\,(e^{U_{ci}/\varphi_{Ti}}-1);$$
$$I_{ci} = \alpha_{Ni}\, I'_{e0i}\,(e^{U_{ei}/\varphi_{Ti}}-1) + (1-e^{U_{ci}/\varphi_{Ti}})\, I'_{c0i}. \tag{1}$$

For a parallel assembly of n transistors, the total voltage U and current $\sum_{i=1}^{n} I_{ci}$ equal

$$U = U_{ei} - U_{ci};\quad \sum_{i=1}^{n} I_{ci} = (E_c - U)/R_L. \tag{2}$$

The power liberated in the i-th transistor is [6]

$$P_i = I_{ci}U + U_{ei}E_b/R_{bi}, \tag{3}$$

where

$$R_{bi} = \begin{cases} R_{b0i}, & T_{s.i} \leqslant T_{cri}, \\ R_{b0i}\,[1 + A_i\,(T_{s.i} - T_{cr.i})], & T_{s.i} > T_{cr.i}; \end{cases} \tag{4}$$

$$I'_{c0i} = I_{c0i}/(1-\alpha_{Ii}\,\alpha_{Ni}),\quad I'_{e0i} = I_{e0i}/(1-\alpha_{Ii}\,\alpha_{Ni}),\quad \varphi_{Ti} = kT_i/q$$

(α_{Ni}, α_{Ii}, I_{c0i}, I_{e0i} are the transistor characteristics).

Solving (1)-(4), we find the currents I_{ci}, the voltages U, U_{ei}, U_{ci} and the heat liberation power P_i of each element as well as the total current of the loads in the loop $\sum_{i=1}^{n} I_{ci}$.

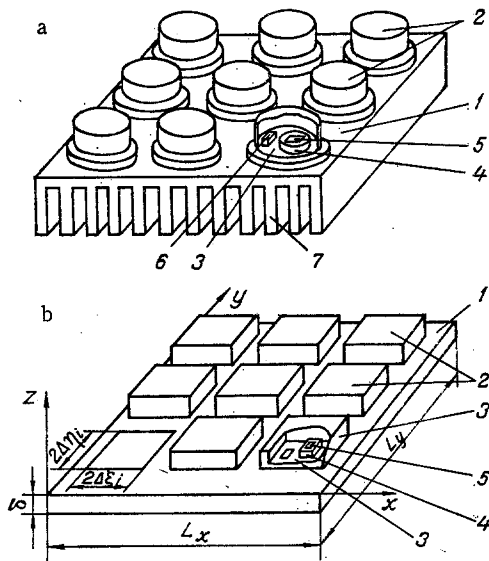

Fig. 2

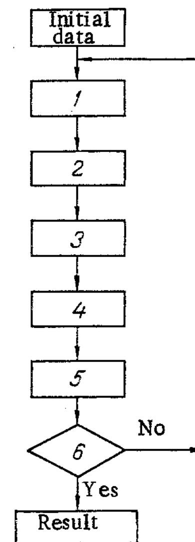

Fig. 3

Fig. 2. Construction (a) and thermal model (b) of a semiconductor module.

Fig. 3. Block diagram for the sequence to compute the thermal and electrical characteristics of a semiconductor gate with a thermal constraint: 1) Compute R_{bi}; 2) analyze the electrical characteristics of the module; 3) determine the heat liberation intensity P_i; 4) compute the module temperature field and the temperature t_{0i} at the sensor attachment point; 5) compute the sensor temperature t_{si}; 6) compare the computed temperature t_{si}^{n} with that tiven in unit 1 t_{si}^{n-1}.

A simplified model of a composite transistor array developed on the basis of the Ebers–Moll model is given in [8].

The thermal model of a gate can be represented in the form of a chassis plate 1 with cells arrayed on it 2, which are in turn modelled by parallelepipeds 4 with local surface heat sources 5 (Fig. 2b). The heat flux liberated in the sources $(P_{3i})_c$ goes into raising the heat content of the parallelepipeds 4, the housing 3, goes through the contact resistance R_{3i}, R_{2i} to the housing 3 and the plate 1 and is dissipated in the medium with open surfaces. Part of the heat flux that has gone into the plate 1 (P_{1i}) goes into raising its heat content and is dissipated in the medium.

According to [4], analysis of such a model is realized in three stages: the temperature field of the chassis 1 with local heat sources P_{1i} is determined in the first stage; the temperature of the cell housings t_{2i} in the second, and the temperature field of the substrate and the semiconductor crystal t_{3i} in the third. Results obtained in the preceding computation stages are initial data in the subsequent analysis via the boundary conditions.

The first model is a plate of dimensions L_x, L_y, δ with local heat sources of intensity P_{1i} with dimensions $2\Delta\xi_{1i}$, $2\Delta\eta_{1i}$ and center coordinates ξ_{1i}, η_{1i}. The heat transfer to the medium occurs from all the surfaces according to Newton's law. The temperature field of the plate is described by the equation

$$c_1\rho_1 \frac{\partial t_1}{\partial \tau} = \lambda_1 \frac{\partial^2 t_1}{\partial x^2} + \lambda_1 \frac{\partial^2 t_1}{\partial y^2} - \frac{\alpha_1 + \alpha_2}{\delta}(t_1 - t_m) + \sum_{i=1}^{n} 1\{I_{1i}\} \frac{P_{1i}}{S_{1i}\delta}, \quad (5)$$

where

$$1\{I_{1i}\} = \begin{cases} 1 \text{ in the domain occupied by the heat source} \\ 0 \text{ outside this domain} \end{cases}$$

under the boundary conditions

$$\lambda_1 \frac{\partial t_1}{\partial j} - \alpha_{j0}(t_1 - t_m)\Big|_{j=0} = 0,$$

$$\lambda_1 \frac{\partial t_1}{\partial j} + \alpha_{j1}(t_1 - t_m)|_{j=L_j} = 0, \quad j = x, y, \tag{6}$$

and the initial condition $t_1(x, y, 0) = t_{10}(x, y)$.

The model in the second stage is a single body 2i (Fig. 2b) with uniform temperature field t_{2i} and total specific heat C_{2i}. The total power P_{2i} being liberated in the element is expended in raising its heat content $C_{2i} \frac{dt_{2i}}{d\tau}$, is dissipated from the housing surface to the medium $\sigma_{2i}(t_{2i} - t_m)$ and partially $(t_{2i} - \bar{t}_{1i})/R_{2i}$ goes through the contact resistance R_{2i} to the plate. On the basis of the energy conservation law, we write the heat balance equation for the body 2i:

$$C_{2i} \frac{dt_{2i}}{d\tau} + (t_{2i} - \bar{t}_{1i})/R_{2i} + \sigma_{2i}(t_{2i} - t_m) = P_{2i} \tag{7}$$

with the initial condition

$$t_{2i}(\tau)|_{\tau=0} = (t_{2i})_0, \tag{8}$$

where

$$\bar{t}_{1i} = \frac{1}{4\Delta\xi_{1i}\Delta\eta_{1i}} \int\limits_{\xi_{1i}-\Delta\xi_{1i}}^{\xi_{1i}+\Delta\xi_{1i}} \int\limits_{\eta_{1i}-\Delta\eta_{1i}}^{\eta_{1i}+\Delta\eta_{1i}} t_{1i}(x, y, \tau)\, dxdy.$$

To determine the temperature field of the element in the third stage, a model is used that represents a parallelepiped with dimensions $(l_{3x})_i$, $(l_{3y})_i$, $(l_{3z})_i$, in contact with the plate 1 or the transistor housing 3 (Fig. 2b). Rectangular heat sources of intensity $(P_{3i})_k$ with sides $2(\Delta\xi_{3i})_k$, $2(\Delta\eta_{3i})_k$ are on its surface. The heat flux goes toward raising the heat content of the parallelepiped $c_{3i}\rho_{3i} \frac{\partial t_{3i}}{\partial \tau}$, goes through the air gap and the contact thermal resistance R_{3i} to the transistor housing; when there is no housing, it is dissipated from the side and upper surfaces of the parallelepiped into the environment with temperature t_c and goes into the plate via the contact thermal resistance. We write the temperature field of the parallelepiped with surface heat sources in the form

$$c_{3i}\rho_{3i} \frac{\partial t_{3i}}{\partial \tau} = (\lambda_{3x})_i \frac{\partial^2 t_{3i}}{\partial x^2} + (\lambda_{3y})_i \frac{\partial^2 t_{3i}}{\partial y^2} + (\lambda_{3z})_i \frac{\partial^2 t_{3i}}{\partial z^2} \tag{9}$$

under the boundary and initial conditions

$$(\lambda_{3x})_i \frac{\partial t_{3i}}{\partial x} \mp (\alpha_{3x})_i (t_{3i} - t^*)|_{x=0,(l_{3x})_i} = 0;$$

$$(\lambda_{3y})_i \frac{\partial t_{3i}}{\partial y} \mp (\alpha_{3y})_i (t_{3i} - t^*)|_{y=0,(l_{3y})_i} = 0;$$

$$(\lambda_{3z})_i \frac{\partial t_{3i}}{\partial z} - (t_{3i} - t^{**})/R_{3i}|_{z=0} = 0;$$

$$(\lambda_{3z})_i \frac{\partial t_{3i}}{\partial z} + (\alpha_{3z})_i (t_{3i} - t^*)|_{z=(l_{3z})_i} = \sum_{k=1}^{K} 1\{(\mathrm{I}_{3i})_k\} \frac{(P_{3i})_k}{4(\Delta\xi_{3i})_k (\Delta\eta_{3i})_k};$$

$$t_{3i}(x, y, z, 0) = [t_{3i}(x, y, z)]_0;$$

$$t^* = \begin{cases} t_m & \text{— for the i-th element without housing} \\ t_{2i} & \text{— for housings present;} \end{cases}$$

$$t^{**} = \begin{cases} \bar{t}_{1i} & \text{— for an element arranged directly on the plate} \\ t_{2i} & \text{— for housings present} \end{cases}$$

$$1\{(I_{3i})_k\} = \begin{cases} 1 - \text{in the domain occupied by the source} \\ 0 - \text{outside this domain} \end{cases}$$

The sensor temperature is governed by the site of its disposition, and the mode and method of fastening. Its magnitude can be found from an analysis of the heat-balance equation: the thermal flux going to the sensor through the contact resistance at the site of its fastening to the object $(t_0 - t_d)/R_{0d}$ goes toward raising the heat content of the sensor $C_s(dt/d\tau)$ and is dissipated in the environment $(t_s - t_m)/R_{sc}$:

$$(t_0 - t_s)/R_{0s} = C_s \frac{dt_s}{d\tau} + (t_s - t_c)/R_{sc}, \tag{11}$$

where t_0 is the temperature of the site where the sensor is fastened. This can be a plate with temperature t_1, housing of the element t_{2i} of transistor crystal t_{3i}.

Therefore, the thermal and electrical processes are determined completely by the combined solution of system (1)-(11).

The block diagram for the computation and joint analysis of the electrical and thermal processes of a transistor assembly based on the models proposed is represented in Fig. 3. Here the initial data are the geometric and thermophysical parameters of the plate and the transistors, the magnitudes of the contact resistances between the transistor and the plate, the housing and the substrate or the semiconductor crystal of the elements; the temperature of the environment, the transistor and the load loop electrical parameters.

The posistor resistance is computed by means of (4) in the first stage (module 1). The temperature is given equal to $T_m = T^I_{si} = T_{cri}$ in a first approximation. Later (module 2) the electrical fields of the apparatus are computed by using the model chosen (1), (2) or [6-8]. The heat liberation intensity P_i of the indentical transistors is computed by means of (3) in module 3. These data are initial data to determine the temperature field of the device (module 4), particularly the temperatures of the semiconductor elements themselves t_{1i}, t_{2i}, t_{3i} and the site in which the thermal sensors (posistors) are located. Then the sensor temperature t_{si} is determined from the relationship (11) in module 5. The quantities of the computed temperature t^n_{si} and that given in the first module t^{n-1}_{si} are compared in module 6, and if their difference is greater than given accuracy ε in modulus, then the computation is performed again until convergence of the iteration cycle.

The temperature fields and electrical characteristics of semiconductor gates were computed by using the method proposed in different operating modes with several variations of the thermal constraint. The data obtained were compared with experiment to determine the error in the computational method and the foundation of the assumptions taken. Tests were performed on six transistors mounted on a common radiator, with element by element thermal protection. The values of the heat liberation intensities in the transistors were determined to a 10-50% error range depending on the mode of transistor operation [6]. The discrepancy between the experimental and computed results was not more than 15% [9], which is satisfactory for engineering purposes.

NOTATION

R_{0bi}, R_{bi}, posistor resistance connected into the base loop of the i-th transistor for $T_i \le T_{cri}$ and $T_i > T_{cri}$, respectively; R_e, resistance in the emitter loop, T_{cri}, critical temperature for posistor actuation; n, quantity of transistors in the parallel assembly; E_b, voltage in the base loop; α_{Ni}, α_{Ii}, gain coefficients of the i-th device; I_{c0i}, I_{e0i}, collector and emitter thermal fluxes of the i-th semiconductor device; U_{ei}, U_{ci}, emitter and collector voltages of the i-th transistor; φ_{Ti}, temperature coefficient of the i-th transistor; k, Boltzmann constant; T_i, temperature of the i-th transistor; q, charge on an electron; I_{ci}, collector current of the i-th transistor; U, total voltage in the transistors; E_c, supply source voltage in the collector loop; R_n, load resistance; P_i, power liberated by the i-th transistor; A_i, slope of the curve $R_{bi} = f(T_i)$; L_x, L_y, δ, plate dimensions; $\Delta\xi_{1i}$, $\Delta\eta_{1i}$, ξ_{1i}, η_{1i}, half the dimensions and the coordinates of the i-th heat source on the plate; $(l_{3x})_i$, $(l_{3y})_i$, $(l_{3z})_i$, dimensions of the i-th parallelepiped-cell; $(\Delta\xi_{3i})_k$, $(\Delta\eta_{3i})_k$, $(\xi_{3i})_k$, $(\eta_{3i})_k$,

half the dimensions and the coordinates of the center of the k-th heat source in the i-th parallelepiped; λ_1, ρ_1, c_1, heat conduction, density, and specific heat of the plate material; $(\lambda_{3x})_i$, $(\lambda_{3y})_i$, $(\lambda_{3z})_i$, ρ_{3i}, c_{3i}, heat conductivity in the appropriate direction, the density and specific heat of the material in the i-th parallelepiped; C_{2i}, total specific heat of the i-th parallelepiped; α_1, α_2, αy_0, αy_1, α_{x_0}, α_{x_1}, heat elimination coefficients from the surfaces of the i-th parallelepiped; R_{2i}, contact thermal resistance between the i-th parallepiped and a plate; R_{3i}, contact thermal resistance between the i-th cell housing and the plate; σ_{ci}, thermal conductivity from the i-th cell to the medium; $t_1(x, y, \tau)$, temperature of body 1; t_{2i}, temperature; $t_{3i}(x, y, z, \tau)$, temperature of the i-th parallelepiped; P_{1i}, part of the heat flux that has passed from the cell into the plate; P_{2i}, total intensity of the heat sources in body 2; $(P_{3i})_k$, heat liberation intensity of the k-th source in the i-th parallelepiped; x, y, z, coordinates; τ, time; t_m, temperature of the environment; R_{os}, R_{sm}, thermal resistance between the object and the temperature sensor, the medium and the sensor; t_o, temperature of the object at the measurement point; t_s, sensor temperature; and C_s, total specific heat of the sensor.

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